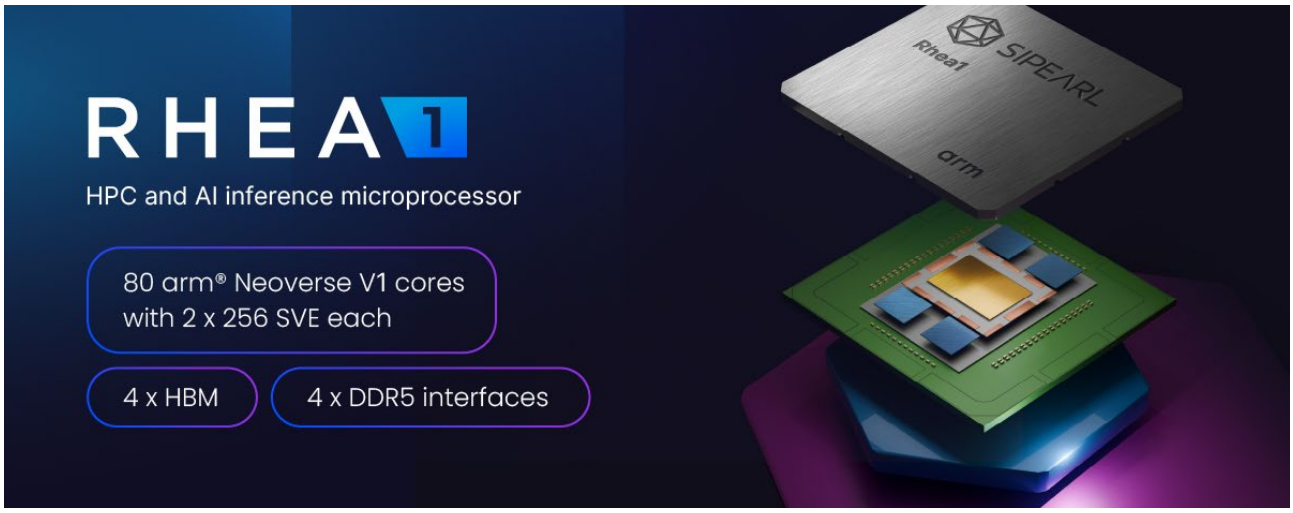
Press release

SiPearl: Rhea1 key features to accelerate HPC & AI inference

SiPearl, the company building the high-performance low-power European microprocessor for HPC[1] and AI inference, unveils the key features of Rhea1, its first-generation product. To meet all the requirements for HPC and AI inference workloads with best-in-class energy-efficiency, Rhea1 will integrate:

- 80 arm® Neoverse V1 cores with 2 Scalable Vector Extension (SVE) units of 256 bits per core,
- built-in High Bandwidth Memory with 4 stacks of HBM,
- 4 DDR5 interfaces.

First samples in 2025.



Maisons-Laffitte (France), May 13, 2024 – Attending ISC tradeshow in Hamburg (booth #L22), SiPearl, the company building the high-performance low-power European microprocessor for HPC and AI inference announces the main features of Rhea1, its first-generation microprocessor.

Designed with high-performance energy-efficient arm® Neoverse V1 platform, Rhea1 will include in a single package:

[1] HPC : High Performance Computing

- 80 arm® Neoverse V1 cores ensuring high compute performance and efficient performance per watt. Each core includes 2 Scalable Vector Extension (SVE) of 256 bits each, enabling fast vector computations while optimizing area and energy use;
- Built-in High Bandwidth Memory, with 4 stacks of HBM, to provide a balanced solution ideal for HPC, big data and AI Inference applications, which are often memory bandwidth bound;
- 4 DDR5 interfaces supporting 2 DIMMs Per Channel (2DPC);
- 104 lanes of PCIe Gen5 interface: up to 6 x16 lanes + 2 x4 lanes;
- High-performance arm® Neoverse CMN-700 Coherent Mesh Network on Chip (NoC) to interconnect compute and I/O elements;
- Support for Flat or Quadrant mode.

Rhea1 is supported by a wide range of compilers, library and tools, from traditional programming languages such as C/C++, GO and RUST to modern AI frameworks such as TensorFlow or PyTorch.

Rhea1 is perfectly suited to traditional HPC workloads - its initial target market - and also to AI inference workloads. Thanks to both the generous memory capacity and high bandwidth of in-package HBM, it will deliver extraordinary performance and energy-efficiency with an unrivalled byte-per-flop ratio.

First samples in 2025.

"*Combining the performance and energy-efficiency of arm® Neoverse V1 cores with in-package HBM and embedding SiPearl patented memory and power management schemes, Rhea1 will fulfill the mission entrusted by EuroHPC JU and the European Processor Initiative consortium: to bring dedicated high-performance microprocessor technologies back to Europe. Rhea1 will be a world class microprocessor for HPC and AI inference. In the fast-growing generative AI market, it will be a great alternative to existing solutions for AI inference workloads at lower cost while offering higher flexibility to model changes*", concluded Philippe Notton, CEO and founder of SiPearl.

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About... SiPearl

SiPearl is building the European high-performance low-power microprocessor dedicated to supercomputing and AI inference. This new generation of microprocessors will first target EuroHPC Joint Undertaking ecosystem, which is deploying world-class supercomputing infrastructures in Europe for solving major challenges in medical research, generative AI, security, energy management and climate with a reduced environmental footprint.

SiPearl is working in close collaboration with its 30 partners from the European Processor Initiative (EPI) consortium - leading names from the scientific community, supercomputing centres and industry - which are its stakeholders, future clients and end-users.

SiPearl employs more than 190 people in France (Maisons-Laffitte, Grenoble, Massy, Sophia Antipolis), Germany (Duisburg), Italy (Bologna) and Spain (Barcelona).

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